Operational Amplifier [Op-Amp]

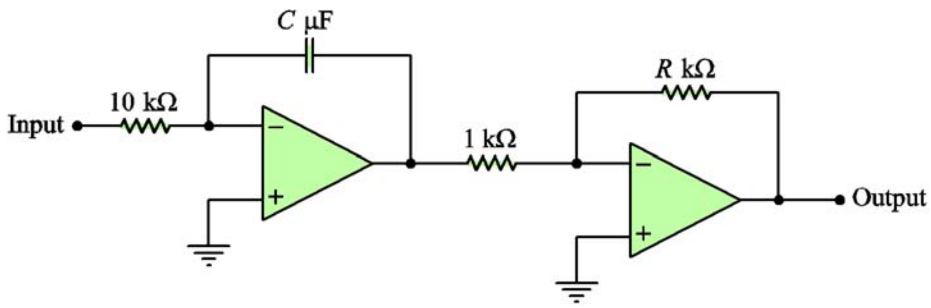
5. OP-AMP APPLICATION (LOGARITHMIC / ANTI-LOGARITHMIC) ANSWER KEYS :

5.1	C	5.2	D	5.3	D	5.4	D	5.5	B
5.6	B								

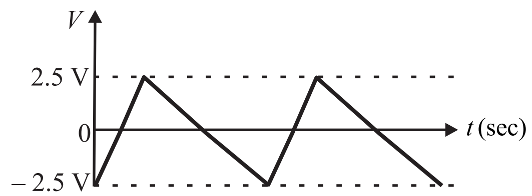
6. OP-AMP APPLICATION (MULTIVIBRATOR / WAVEFORM GENERATOR) ANSWER KEYS :

6.1	B	6.2	C	6.3	C	6.4	A	6.5	C
6.6	B	6.7	D	6.8	A	6.9	A	6.10	C
6.11	0.635	6.12	0.8	6.13	A	6.14	A	6.15	0.798

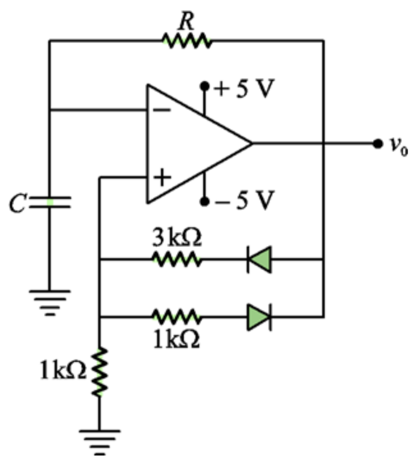
6.6 **Correction**



6.7 **Correction option (D)**



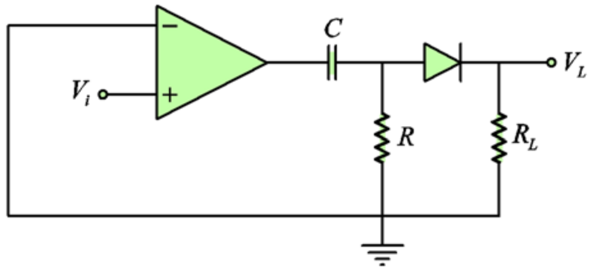
6.12 **Correction**



7. OP-AMP APPLICATION (RECTIFIER / PEAK DETECTOR / CLIPPER / CLAMPER) ANSWER KEYS :

7.1	B, C	7.2	*	7.3	B	7.4	D	7.5	D
7.6	D	7.7	B	7.8	A	7.9	B	7.10	D
7.11	C	7.12	1.6	7.13	A	7.14	B		

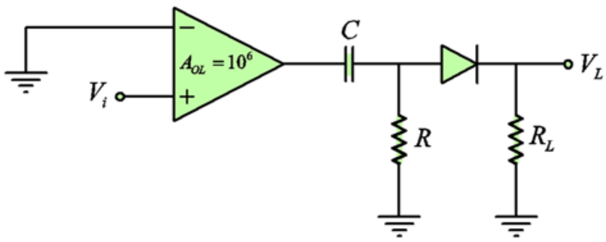
7.5 Op-Amp circuit shown in the given figure is **[IES EC 1995]**



(A) a sample and hold circuit (B) An integrator
(C) A zero crossing detector (D) A half-wave precision rectifier

Ans. (D)

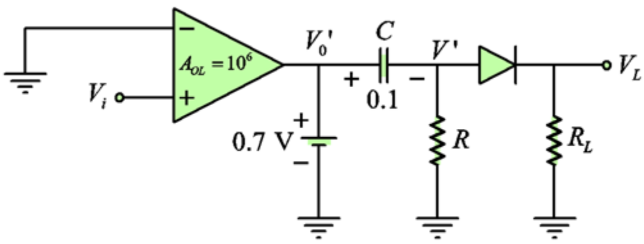
Sol. Modified circuit is shown below,
Assuming open loop gain $A_{OL} = 10^6$



1. For $V_i > 0$, ($V_i = 0.7\ \mu$V)

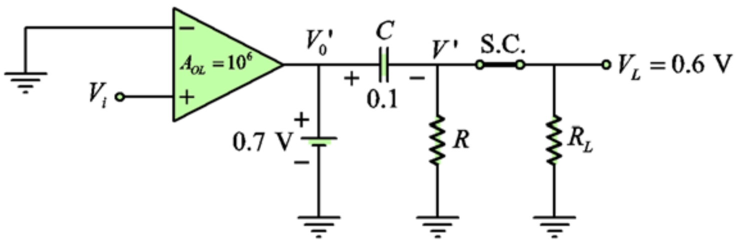
$$V_0' = A_{OL} V_i$$

$$V_0' = 10^6 \times 0.7 \times 10^{-6} = 0.7 \text{ V}$$



Let capacitor charges with small voltage 0.1 V.
Applying KVL, $-0.7 + 0.1 + V' = 0$

$$V' = 0.6 \text{ V} \quad \Rightarrow \quad D \text{ is ON}$$

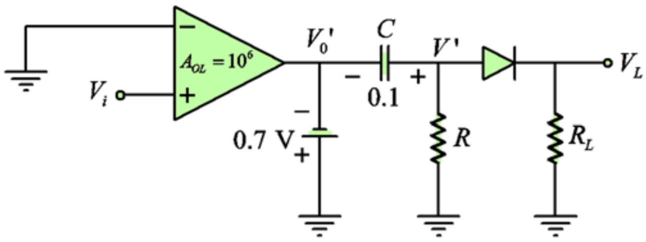


$V_L \approx A_{OL} V_i$ (Capacitor takes some voltage)

2. For $V_i < 0$, ($V_i = -0.7\ \mu$V)

$$V_0' = A_{OL} V_i$$

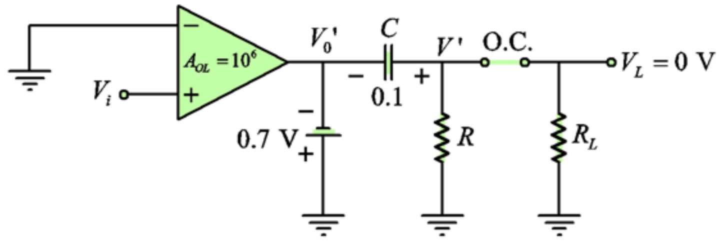
$$V_0' = 10^6 \times (-0.7 \times 10^{-6}) = -0.7 \text{ V}$$



Let capacitor charges with small voltage – 0.1 V.

Applying KVL, $0.7-0.1+V'=0$

$V'=-0.6\text{ V} \Rightarrow$ D is OFF



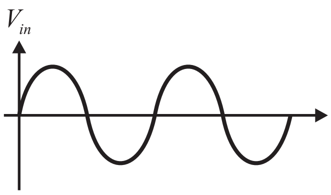
$V_L=0\text{ V}$

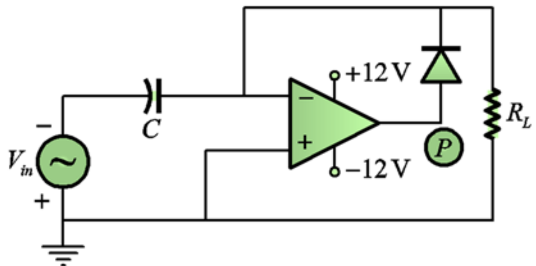
In positive half cycle $V_L=A_{OL}V_i$

In negative half cycle $V_L=0$

Hence it is a half wave rectifier circuit. Since for small value of input ($0.7\ \mu\text{V}$) we get output. Hence it is a precision half wave rectifier circuit.

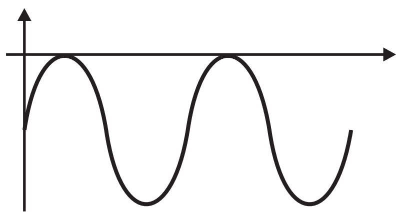
7.6 For a given sinusoidal input voltage, the voltage waveform at point P of the clamper circuit shown in figure will be **[GATE EE 2006, IIT-Kharagpur]**



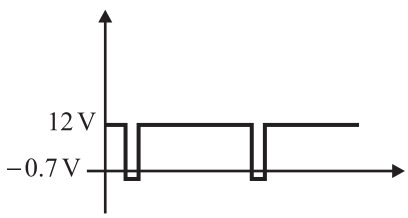


(A)

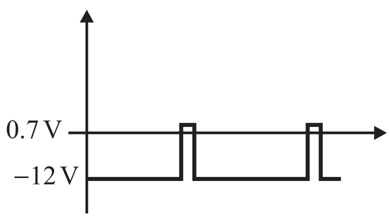
(B)



(C)

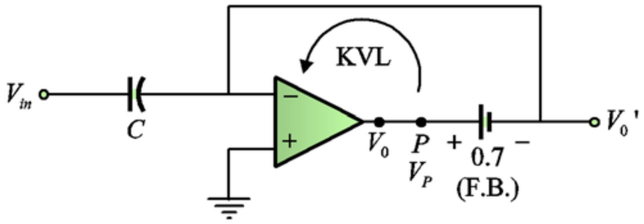


(D)



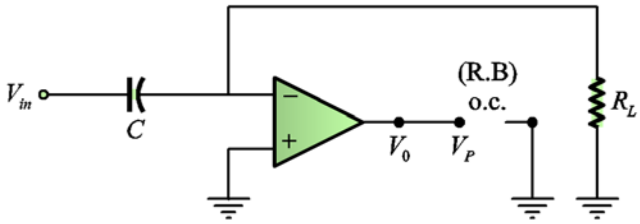
Ans. (D)

Sol. **Case I :** During negative half cycle of input, output of *op*-amp $V_0=+V_{sat}$ and diode D is forward biased.

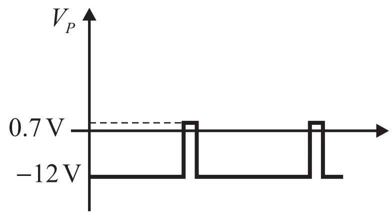


$$\boxed{V_p = 0.7\,\text{V}}$$

Case II : During positive half cycle of input, output of op-amp $V_0 = -V_{sat}$ and diode is reversed biased

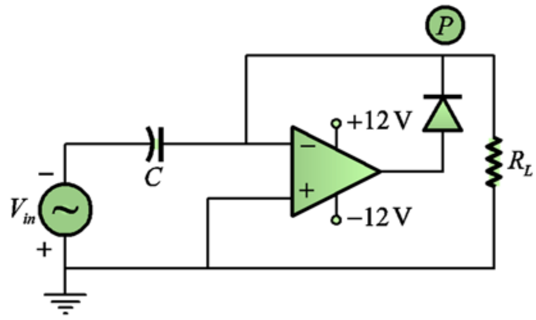


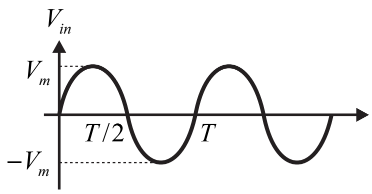
$$\boxed{V_p = -12\text{ V}}$$



Hence the correct option is (D).

If position of P is changed





For positive half cycle

At $t = \dfrac{T}{4}$, $V_{in} = V_m$

Then NI > I

So $V_0 = +V_{sat}$, diode is ON

Capacitor will charge up to $V_C = V_{sat} - (-V_m) = V_{sat} + V_m$

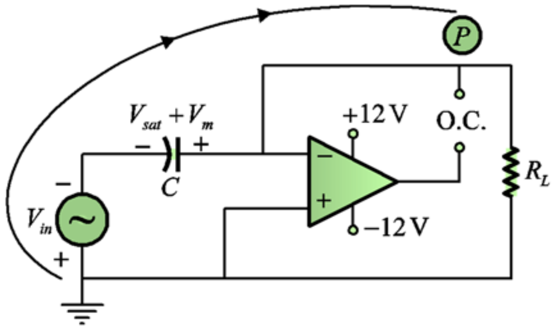
And capacitor will hold this voltage due to high value of load resistance

At $t = \dfrac{3T}{4}$

$$V_p = V_{sat} + 2V_m$$

In the next negative half cycle V_p will discharge up to $+V_{sat}$

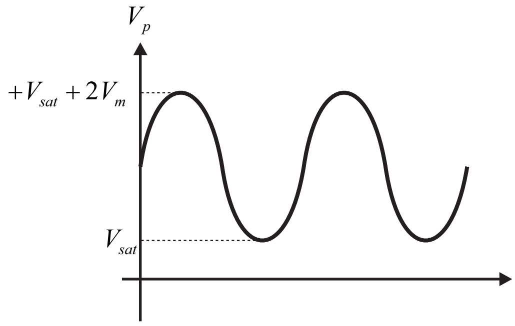
So diode is OFF



Applying KVL in the loop shown

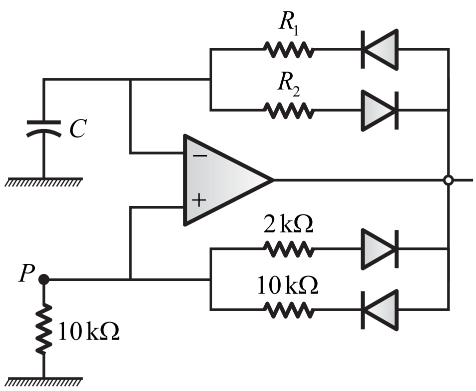
$$+V_{in}-(V_{sat}+V_m)+V_p=0$$

$$V_p=V_{sat}+V_m-V_{in}$$

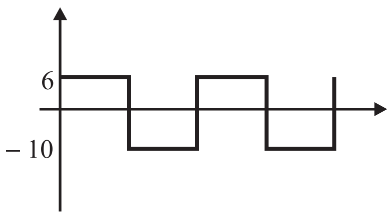


In this case circuit behaves as a positive clamper.

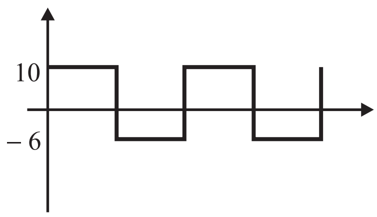
7.8 A relaxation oscillator is made using Op-Amp as shown in below figure. The supply voltages of the Op-Amp are $\pm 12\text{ V}$. The voltage waveform at point P will be **[GATE EE 2006, IIT-Kharagpur]**



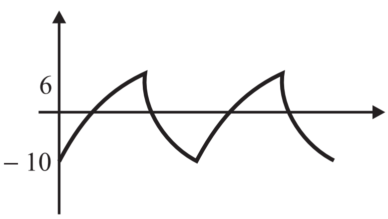
(A)



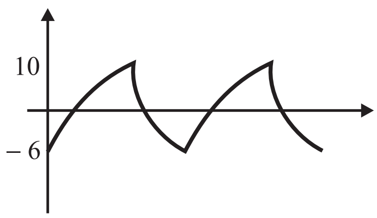
(B)



(C)

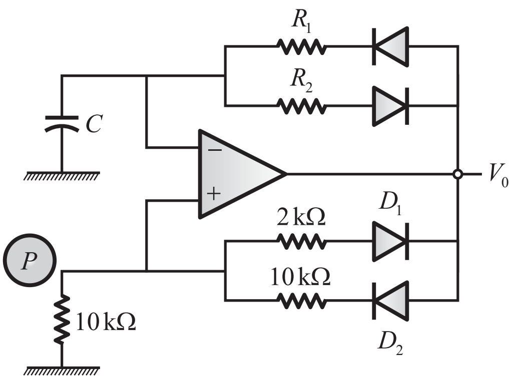


(D)



Ans. **(C)**

Sol. **Given :** A relaxation oscillator



Output voltage of relaxation oscillator mode using op- amp will switch + 12 V and – 12 V

When $V_0 = +12$ V, diode D_2 will be forward biased

$$\therefore \qquad V_p = +12 \times \frac{10}{10+10}$$

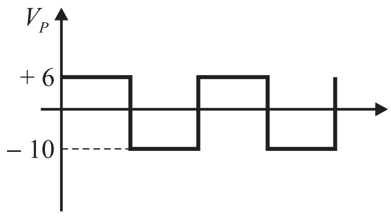
$$\therefore \qquad \boxed{V_p = +6 \text{ V}}$$

when $V_0 = -12$ V, diode D_1 will be forward biased

$$V_p = -12 \times \frac{10}{10+2}$$

$$\therefore \qquad \boxed{V_p = -10 \text{ V}}$$

Therefore the voltage waveform at point P



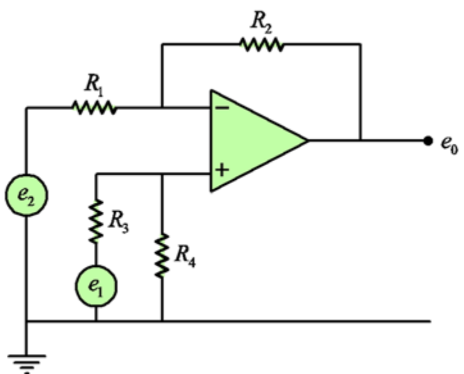
8. OP-AMP CHARACTERISTICS (SLEW RATE) ANSWER KEYS :

8.1	D	8.2	C	8.3	159	8.4	B	8.5	C
8.6	A	8.7	B	8.8	C	8.9	A	8.10	D
8.11	A	8.12	B	8.13	D	8.14	C	8.15	B
8.16	D	8.17	B						

9. OP-AMP CHARACTERISTICS (CMRR) ANSWER KEYS :

9.1	C	9.2	A	9.3	$V_{cm} = V_0$	9.4	140	9.5	D
9.6	D	9.7	C	9.8	B	9.9	D	9.10	A
9.11	B	9.12	A	9.13	C	9.14	D	9.15	40.4

9.5 Correction

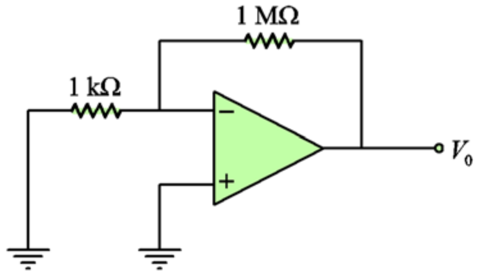


10. OP-AMP CHARACTERISTICS (BIAS / OFFSET) ANSWER KEYS :

10.1	C	10.2	D	10.3	D	10.4	B	10.5	D
10.6	C	10.7	D	10.8	A	10.9	C	10.10	C
10.11	C	10.12	D	10.13	C	10.14	D	10.15	413.8
10.16	20								

10.1 An op amp has an offset voltage of 1 mV and is ideal in all other respects. If this op amp is used in the circuit shown in the given figure, the output voltage will be (select the nearest value).

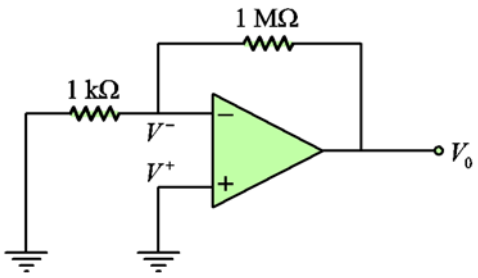
[GATE EC 1992, IIT-Delhi]



(A) 1 mV (B) 1 V (C) ± 1 V (D) 0 V

Ans. (C)

Sol.



$$V_{ios} = V^+ - V^-$$

If $V^+ = 1$ mV and $V^- = 0$

$\Rightarrow$ $V_{ios} = 1$ mV

$$V_0 = \left[1 + \frac{R_f}{R}\right] V_{ios}$$

$$V_0 = \left[1 + \frac{10^3}{1}\right] 1 = 1 \text{ V}$$

If $V^- = 1$ mV and $V^+ = 0$

$\Rightarrow$ $V_{ios} = -1$ mV

$$V_0 = \left[1 + \frac{R_f}{R}\right] V_{ios}$$

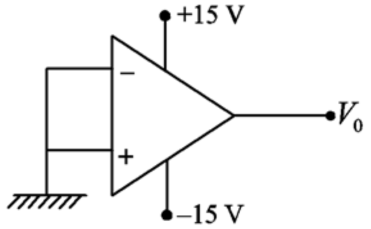
$$V_0 = \left[1 + \frac{10^3}{1}\right] (-1) = -1 \text{ V}$$

So $V_0 = \pm 1$ V

Key point :

If option has + 1 and – 1 V then we will prefer + 1 V.

10.6 If the Op-Amp in given figure, has an input offset voltage of 5 mV and an open-loop voltage gain of 10,000, then V_0 will be **[GATE EC 2000, IIT-Kharagpur]**



(A) 0 V (B) 5 mV
(C) +15 V or – 15 V (D) + 50 V or – 50 V

Ans. (C)

Sol. $V_{OOS} = A_{ios} \times A_{OL}$

$V_{OOS} = 5 \times 10^{-3} \times 10^{4} = 50 \text{ V (saturated)}$

$V_{OOS} = \pm 15 \text{ V}$

11. OP-AMP APPLICATION (INSTRUMENTATION AMPLIFIER) :

11.1	B	11.2	D	11.3	C	11.4	A	11.5	A

12. OP-AMP APPLICATION (SAMPLE AND HOLD CIRCUIT) ANSWER KEYS :

12.1	5×10^{-3}	12.2	B	12.3	C	12.4	D	12.5	B
12.6	B								

13. OP-AMP APPLICATION (REGULATOR) ANSWER KEYS :

13.1	C	13.2	C	13.3	D	13.4	B	13.5	C
13.6	1092 – 1094	13.7	2.8	13.8	1.145				

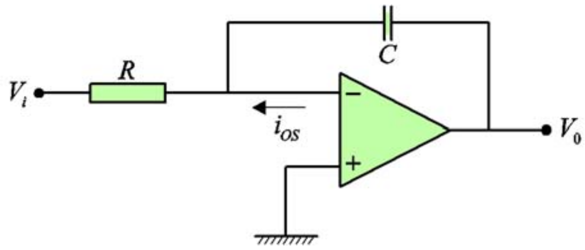
14. DIFFERENTIAL AMPLIFIER ANSWER KEYS :

14.1	B	14.2	B	14.3	A	14.4	A	14.5	C
14.6	A	14.7	B	14.8	A	14.9	B	14.10	D
14.11	A	14.12	C	14.13	A	14.14	B	14.15	B
14.16	1.5								

15. MISCELLANEOUS ANSWER KEYS :

15.1	A	15.2	B	15.3	A	15.4	B	15.5	C
15.6	D	15.7	A	15.8	D	15.9	A	15.10	B
15.11	C	15.12	D	15.13	D	15.14	D	15.15	A
15.16	A	15.17	A	15.18	C	15.19	B	15.20	D
15.21	A	15.22	D	15.23	D	15.24	B	15.25	D
15.26	D	15.27	B	15.28	C	15.29	B	15.30	C
15.31	D	15.32	B	15.33	D	15.34	B	15.35	C
15.36	D	15.37	B	15.38	A	15.39	C	15.40	D
15.41	B	15.42	B	15.43	3	15.44	800	15.45	C
15.46	C								

15.13 An integrator circuit is shown in below figure. The Op-Amp is of type 741 and has an input offset current i_{os} of $1\ \mu A$. C is $1\mu F$ and R is $1\ M\Omega$. If the input V_i is a 1 kHz square wave of 1 V peak to peak, the output V_0, under steady state condition, will be **[GATE IN 2003, IIT-Madras]**



(A) a square wave of 1 V peak to peak

(B) a triangular wave of 1 V peak to peak

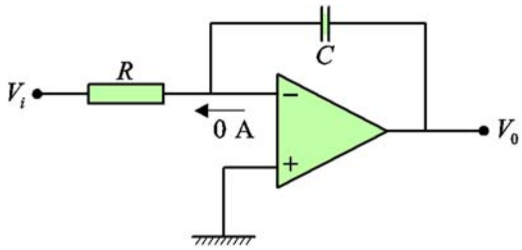
(C) positive supply voltage $+V_{CC}$

(D) negative supply voltage $-V_{CC}$

Ans. (D)

Sol. By Super position theorem

1. Consider voltage source V_i, $(i_{OS}=0)$



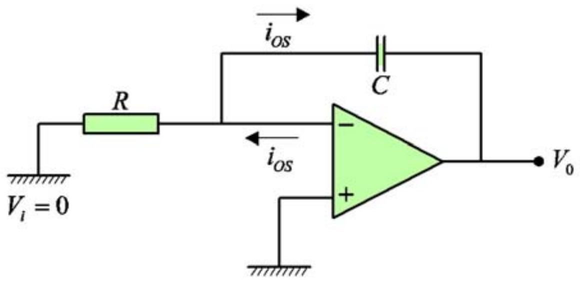
Time constant, $\tau = RC = 10^6 \times 10^{-6} = 1$ sec

V_i is a 1 kHz square wave of 1 V peak to peak. So time period $T = \frac{1}{f} = \frac{1}{1\text{ kHz}} = 1$ msec

Input changes very quickly so capacitor does not have enough time to charge or discharge.

So $V_C = 0 \Rightarrow V_0 = 0$ V

2. Consider only i_{OS}, $(V_i = 0)$



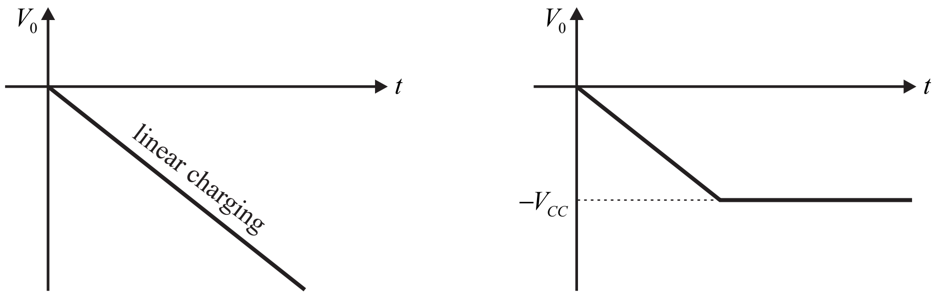
$$i_{OS} = C\frac{d}{dt}(0 - V_0)$$

$$i_{OS} = -C\frac{d}{dt}V_0$$

$$V_0 = -\frac{1}{C}\int i_{OS}\,dt$$

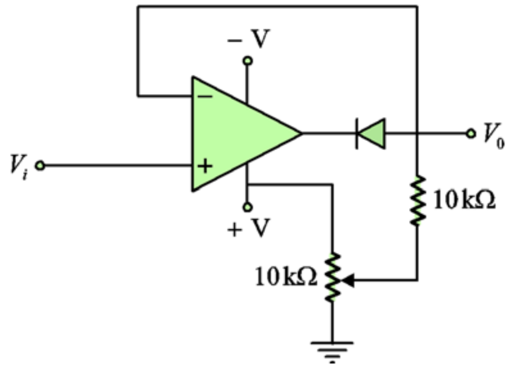
$$V_0 = \frac{-10^{-6}}{10^{-6}}\int dt \qquad [C = 1\ \mu F,\ i_{OS} = 1\ \mu A]$$

$$V_0 = -t$$



Output of Op-Amp lies between $+V_{CC}$ and $-V_{CC}$. So V_0 saturate at $-V_{CC}$.

15.18 Consider the following circuit **[IES EC 2004]**



How does the below circuit work?

(A) As a logarithmic amplifier

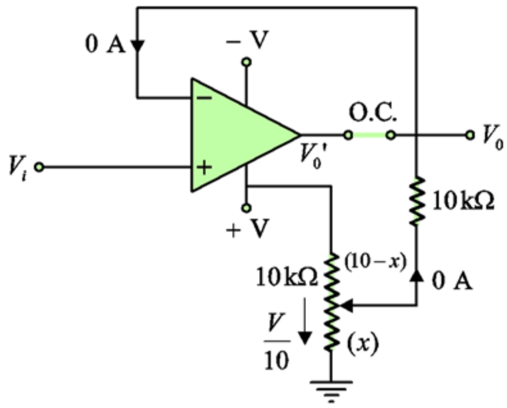
(B) As a negative clipper

(C) As a positive clipper

(D) As a half-wave rectifier

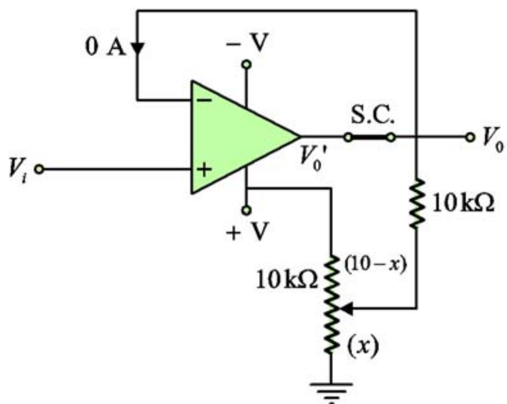
Ans. **(C)**

Sol. For $V_i > 0$, $V_0' = +V$ $\Rightarrow$ D is OFF

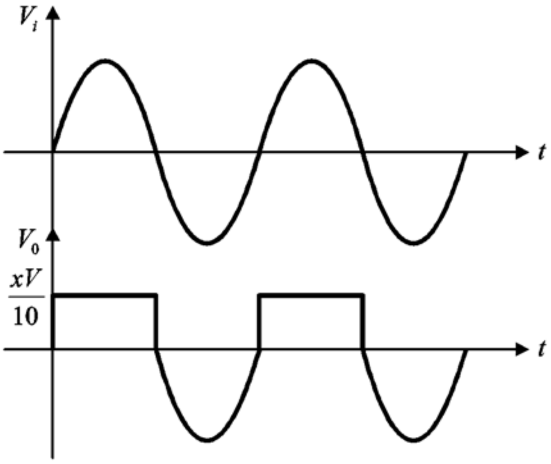


From figure $V_0 = \frac{xV}{10}$ (constant)

For $V_i < 0$, $V_0' = -V$ $\Rightarrow$ D is ON

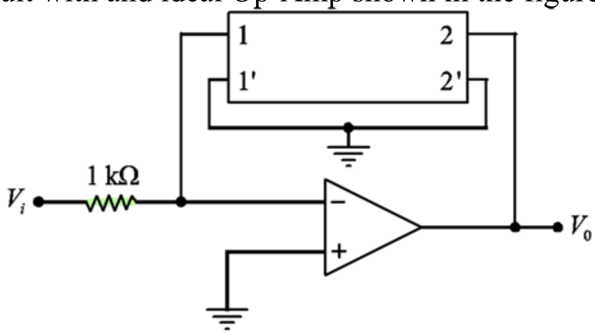


Voltage follower circuit $V_0 = V_i$.



Since maximum positive portion at output gets clipped hence the circuit is clipper circuit.

15.26 Consider the linear circuit with and ideal Op-Amp shown in the figure below.



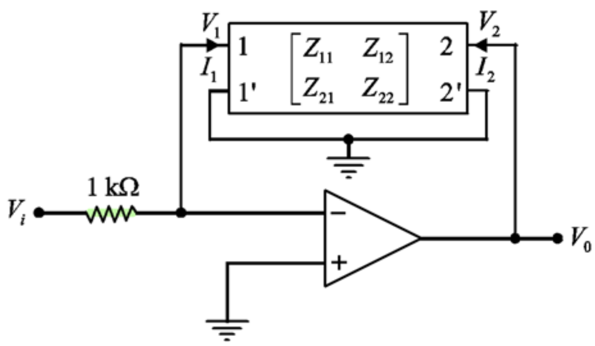
The Z-parameters of the two port feedback network are $Z_{11} = Z_{22} = 11\ \text{k}\Omega$ and $Z_{12} = Z_{21} = 1\ \text{k}\Omega$

The gain of the amplifier is **[GATE IN 2007, IIT-Kanpur]**

(A) + 110 (B) + 11 (C) – 1 (D) – 120

Ans. **(D)**

Sol.



Given : Z-parameter $= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 11 & 1 \\ 1 & 11 \end{bmatrix}$ ……. (i)

Standard Z-parameter equation is given by,

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

So, from equation (i),

$$V_1 = 11I_1 + I_2 \quad \text{...... (ii)}$$

$$V_2 = I_1 + 11I_2 \quad \text{....... (iii)}$$

$$V_1 = 0 \quad \text{[From VGC]}$$

From equation (ii),

$$11I_1 + I_2 = 0$$

$$I_2 = -11I_1 \quad \text{....... (iv)}$$

$$V_0 = V_2 \quad \text{[From figure]}$$

From equation (iii),

$$V_0 = I_1 + 11I_2$$

$$V_0 = I_1 + 11(-11I_1) \qquad \text{[From equation (iv)]}$$

$$V_0 = -120I_1$$

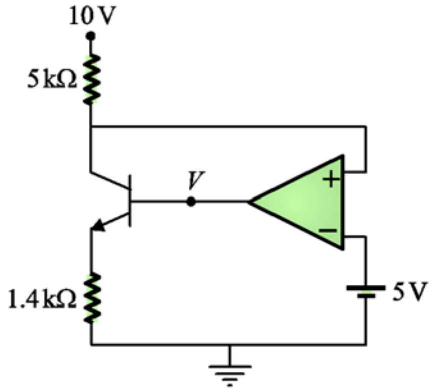
Applying KCL at inverting terminal

$$I_1 = \frac{V_i}{1} \Rightarrow \quad V_i = I_1$$

So, $$V_0 = -120V_i$$

$$\text{Gain} = \frac{V_0}{V_i} = -120$$

15.31 In the circuit shown below, the Op-Amp is ideal, the transistor has $V_{BE} = 0.6$ V and $\beta = 150$. Decide whether the feedback in the circuit is positive or negative and determine the voltage V at the output of the Op-Amp. **[GATE EC 2009, IIT-Roorkee]**

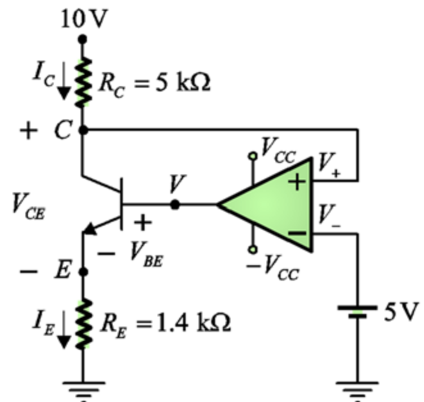


(A) Positive feedback, V = 10 V (B) Positive feedback, V = 0 V

(C) Negative feedback, V = 5 V (D) Negative feedback, V = 2 V

Ans. (D)

Sol.



Let us first assume that there is a positive feedback. Then V can either $+V_{CC}$ or $-V_{CC}$.

Let $V_{CC} = 10$ V

Now, for there to be a feedback, transistor must be ON.

V can not be $-V_{CC}$

$$V = +V_{CC} = +10 \text{ V}$$

Applying KVL in emitter loop :

$$V - V_{BE} - I_E R_E = 0$$

$$I_E = \frac{10 - 0.6}{1.4} = 6.7 \text{ mA}$$

$$I_C \approx I_E = 6.7 \text{ mA} \quad [\beta \text{ is large}]$$

$$V_C = 10 - I_C R_C = 10 - 6.7 \times 5$$

$$V_C = -23.5 \text{ V}$$

$$V_E = I_E R_E = 9.6 \text{ V}$$

$V_{CE} < 0$ or CB junction is forward biased

The transistor is in saturation region.

$$V_{CE} = V_{CE,\,sat} = 0.2 \text{ V} \quad [\text{say}]$$

$$10 - I_C R_C - V_{CE} - I_E R_E = 0$$

So,
$$I_C \simeq I_E = \frac{10 - 0.2}{R_C + R_E} = \frac{9.8}{5 + 1.4}$$

$$I_C \simeq I_E = 1.53 \text{ mA}$$

$$V_C = 10 - I_C R_C$$

$$V_C = 10 - 1.53 \times 5 = 2.65 \text{ V}$$

$$V_+ = V_C = 2.65 \text{ V}$$

But $V_- = 5$ V

$$V_+ < V_-$$

$$V = -V_{CC}$$

But we assumed that $V = +V_{CC}$

Hence there can't be positive feedback.

Therefore Op-Amp will be in negative feedback.

Then
$$V_+ = V_- = 5 \text{ V} \quad [\text{From VGC}]$$

$$V_C = +5 \text{ V}$$

$$I_C = \frac{10 - V_C}{R_C} = \frac{10 - 5}{5} = 1 \text{ mA}$$

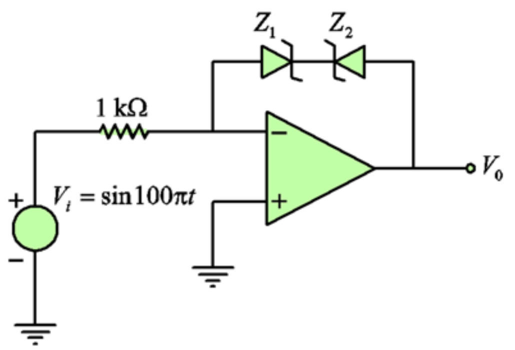
$$I_E \approx I_C = 1 \text{ mA}$$

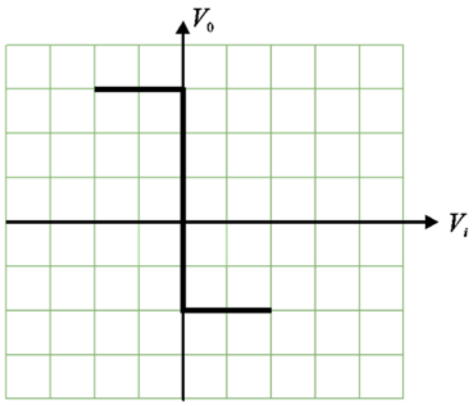
$$V = V_{BE} + I_E R_E$$

$$V = 0.6 + 1 \times 1.4 = 2 \text{ V}$$

Hence, there will be a negative feedback with $V = 2$ V.

15.36 The transfer characteristic of the circuit drawn below is observed on an oscilloscope used in XY mode. The display on the oscilloscope is shown on the right hand side. V_i is connected to the X input with a setting of 0.5 V/div, and V_0 is connected to the Y input with a setting of 2 V/div. The beam is positioned at the origin when V_i is zero. **[GATE IN 2011, IIT-Madras]**



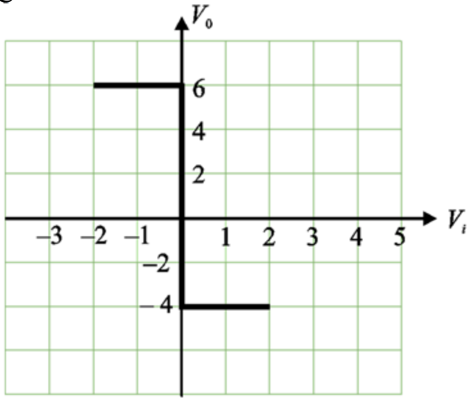


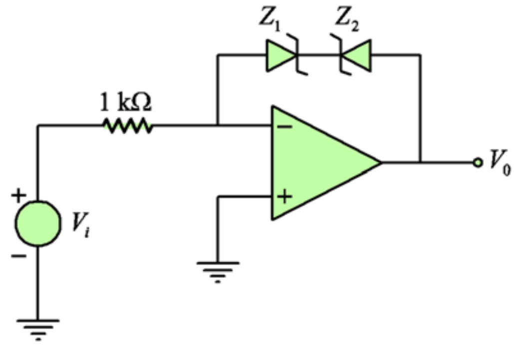
Assuming that is the Op-Amp is ideal an the zener diodes have forward biased voltage drop of 0.7 V, the values of reverse break-down voltages of Z_1 and Z_2 are, respectively,

(A) 3.3 V and 5.3 V
(B) 4.7 V and 6.7 V
(C) 6.7 V and 4.7 V
(D) 5.3 V and 3.3 V

Ans. (D)

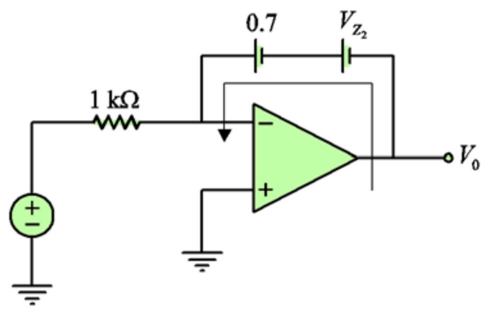
Sol. V_i is connected to the X input with a setting of 0.5 V/div, and V_0 is connected to the Y input with a setting of 2 V/div. So the transfer characteristics can be modified as





When V_i is +ve then Z_1 is F.B. and Z_2 is R.B. so replace Z_1 by forward voltage drop.

When V_i is + ve, then $V_{out} = -4$ Volts (from graph)



Applying KVL in the loop shown

$$-V_0 - V_{Z_2} - 0.7 = 0$$

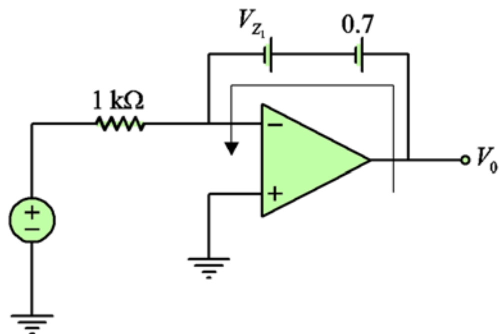
$$V_0 = -V_{Z_2} - 0.7$$

$$-4 = -V_{Z_2} - 0.7$$

$$V_{Z_2} = 3.3 \text{ V}$$

When V_i is –ve then Z_1 is RB and Z_2 is FB.

So replace Z_2 by forward voltage drop and when $V_i = -$ ve $V_{out} = 6$ volts (From graph)



Applying KVL in the loop shown

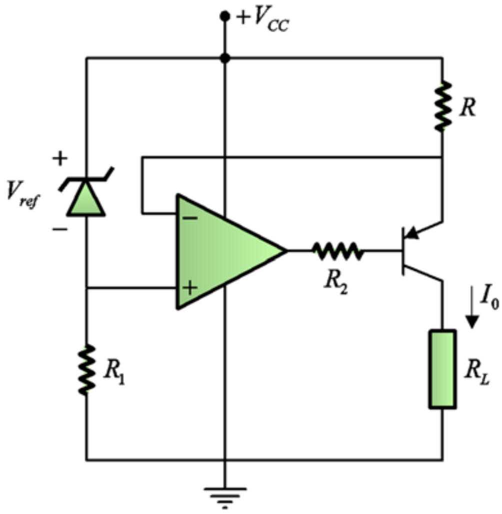
$$-V_0 + V_{Z_1} + 0.7 = 0$$

$$V_0 = 0.7 + V_{Z_1}$$

$$6 = 0.7 + V_{Z_1}$$

$$V_{Z_1} = 5.3 \text{ V}$$

15.42 Correction



15.45 The transient response rise time (unity gain) of an Op-Amp is 0.05 μs. The small signal bandwidth is **[IES EC 2016]**

(A) 7 kHz (B) 20 kHz (C) 7 MHz (D) 20 MHz

Ans. (C)

Sol. Rise time in terms of bandwidth is given by,

$$t_r = \frac{0.35}{\text{B.W.}}$$

$$\text{Bandwidth } = \frac{0.35}{t_r} = \frac{0.35}{0.05\ \mu\text{s}} = \frac{35}{5} \times 10^6 \text{ Hz} = 7 \text{ MHz}$$

PRACTICE TEST - 01 ANSWER KEYS :

1.	1.5	2.	C	3.	210	4.	B	5.	B
6.	40	7.	D	8.	–11	9.	245	10.	8
11.	C	12.	2	13.	6	14.	–5	15.	610
16.	–5	17.	–1	18.	B	19.	A	20.	A
21.	2	22.	C	23.	A	24.	6	25.	D

PRACTICE TEST - 02 ANSWER KEYS :

1.	–2.5	2.	D	3.	A	4.	C	5.	B
6.	A	7.	D	8.	A	9.	C	10.	B
11.	B	12.	B	13.	B	14.	2.4	15.	C
16.	C	17.	C	18.	B	19.	D	20.	C
21.	B	22.	C	23.	B	24.	A	25.	A
26.	C	27.	D	28.	B	29.	A	30.	37.78